Notice of Allowability	Application No.	Applicant(s)	
	10/617,040	ITO ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview 1/24/2007*.

2. ☒ The allowed claim(s) is/are *1-7 and 9-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/26/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *1/24/2007* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1/24/07

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with Francis G. Plati, Sr. on Wednesday, January 24, 2007.

Please amend the application as follows:

Please replace claim 1 with:

1. (currently amended): A semiconductor memory device comprising:

an SDRAM array made up of a plurality of memory cells and having an information bit area wherein information bits are written in and / or read from and a parity bit area wherein parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in at least one of said information bits and said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code on data including said information bits and said parity bits being written in and /or read from said information bit area and said parity bit area, respectively, in said SDRAM array,

wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and

wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals.

Please replace claim 2 with:

2. (currently amended): The semiconductor memory device according to Claim 1, wherein, when reading process is performed on said information bit area or said parity bit area, said read data on which said error correcting processing has been performed is output to only an outside of said SDRAM array without being rewritten into said information bit area or said parity area.

Please replace claim 3 with:

3. (currently amended): The semiconductor memory device according to Claim 1, wherein, when a codeword made up of bits is beyond a correcting capability of said error correcting processing using said Hamming Code, said redundant correction processing is performed on said error bits using said redundant circuit.

Please replace claim 9 with:

9. (currently amended): A semiconductor memory device comprising:

an SDRAM array made up of a plurality of memory cells and having an information bit area wherein information bits are written in and / or read from and a parity bit area wherein parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in at least one of said information bits and said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code whose code length is 72 or less on data including said information bits and said parity bits being written in and /or read from said information bit area and said parity bit area, respectively, in said SDRAM array,

wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and

wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals.

Please replace claim 10 with:

10. (currently amended): The semiconductor memory device according to Claim 9, wherein, when reading process is performed on said information bit area or said parity bit area, said read data on which said error correcting processing has been performed is output to only an outside of said SDRAM array without being rewritten into said information bit area or said parity area.

Please replace claim 11 with:

11. (currently amended): The semiconductor memory device according to Claim 9, wherein, when a codeword made up of bits is beyond a correcting capability of said error correcting processing using said Hamming Code, said redundant correction processing is performed on said error bits using said redundant circuit.

REASONS FOR ALLOWANCE

Claims 1-7 and 9-15 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a semiconductor memory device comprising: an SDRAM array made up of a plurality of memory cells and having an information bit area wherein information bits are written in and / or read from and a parity bit area wherein parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in at least one of said information bits and said parity bits; and an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code on data including said information bits and said parity bits being written in and /or read from said information bit area and said parity bit area, respectively, in said SDRAM array, wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data

mask block and controlled by independent data mask signals as external signals. The foregoing limitations are not found in the prior arts of record. Particularly, none of the prior arts of record teach nor fairly suggest, *"...wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals."*

Independent claim 9 includes similar limitations of independent claim 1 and therefore is allowed for similar reasons.

Dependent claims 2-7 and 10-15 depend from allowable independent claims 1 and 9 and inherently include limitations therein and therefore are allowed as well.

Conclusion

The duplicate references on the IDS submitted October 26, 2006 has been considered in view of Applicants' remarks referring to the statement of relevance provided in the IDS submitted July 07, 2006.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mujtaba Chaudry
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January 24, 2007